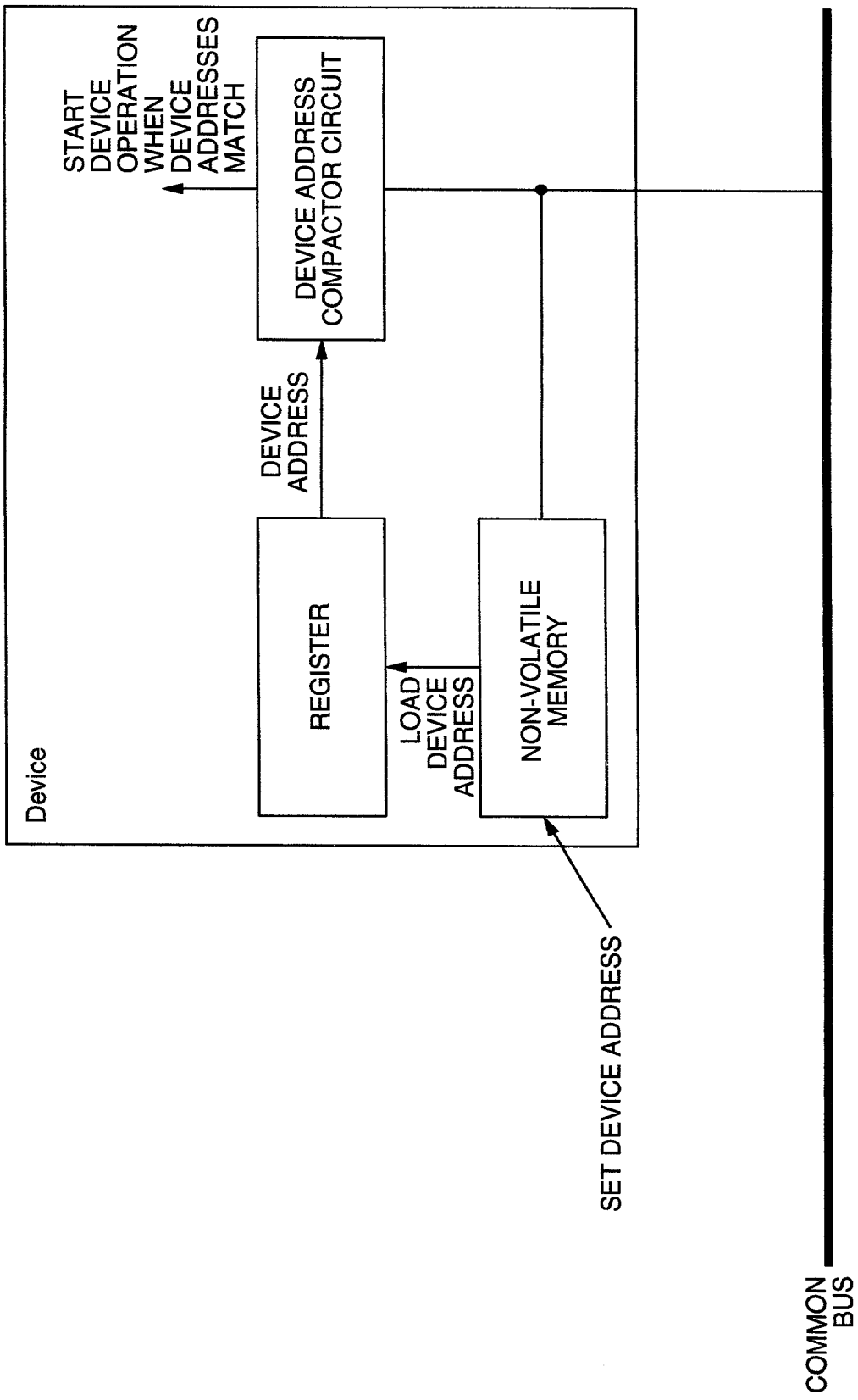
Patent Technology

FIG. 1



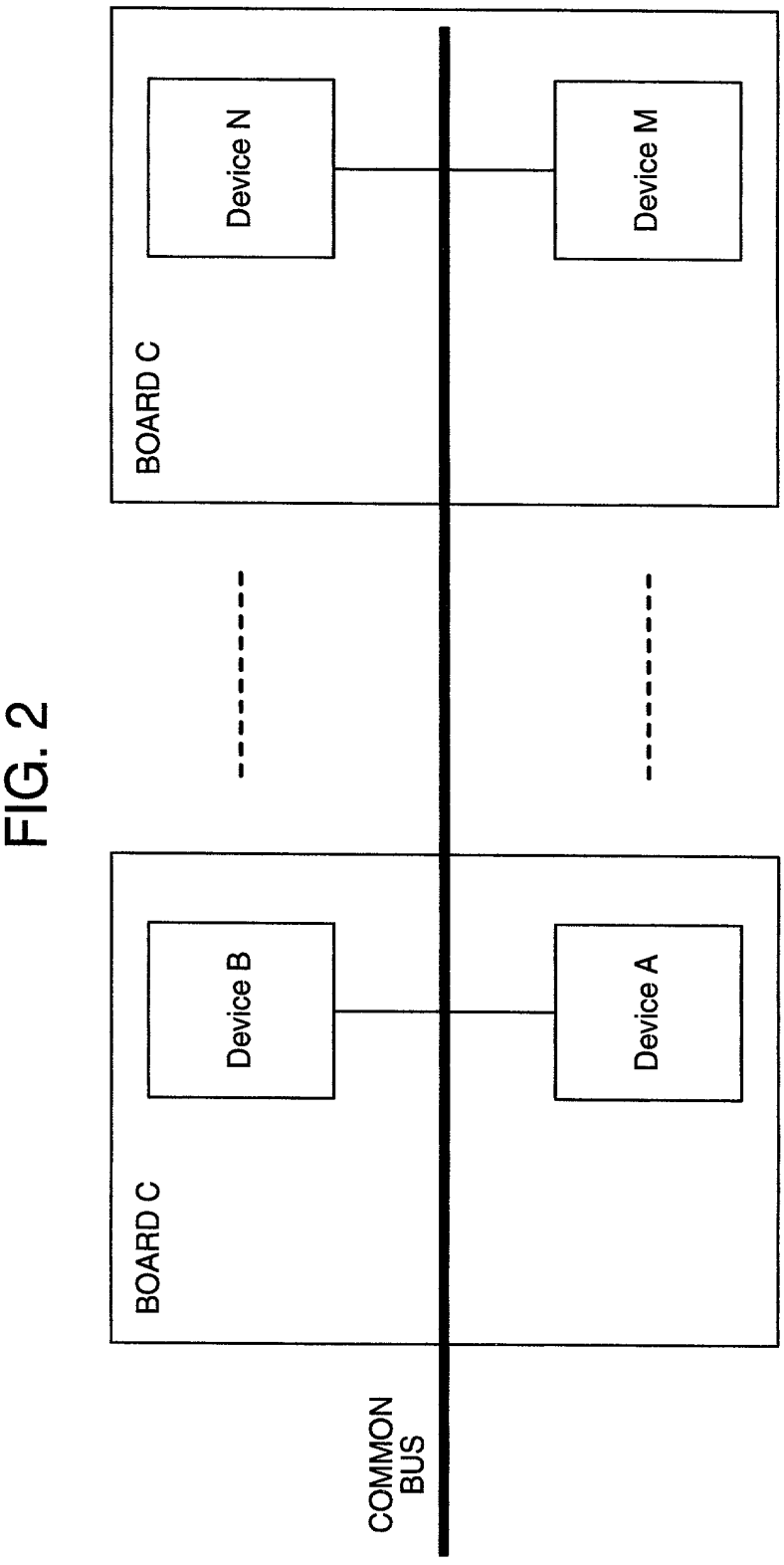
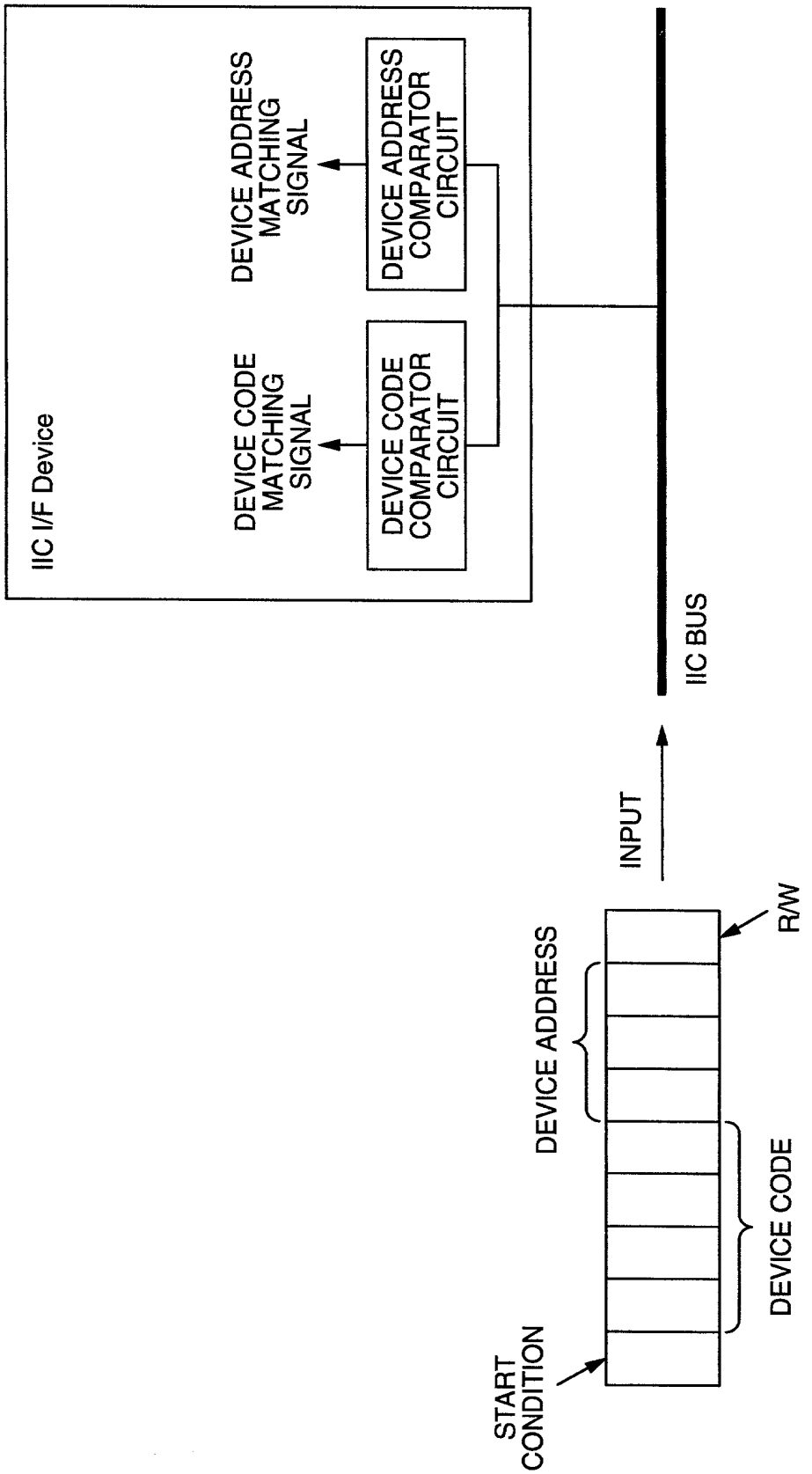


FIG. 2

FIG. 3


IIC I/F Device
DEVICE CODE COMPARATOR CIRCUIT
DEVICE ADDRESS COMPARATOR CIRCUIT
DEVICE CODE MATCHING SIGNAL
DEVICE ADDRESS MATCHING SIGNAL
IIC BUS
INPUT
START CONDITION
DEVICE CODE
DEVICE ADDRESS
R/W

Patent Application

FIG. 4

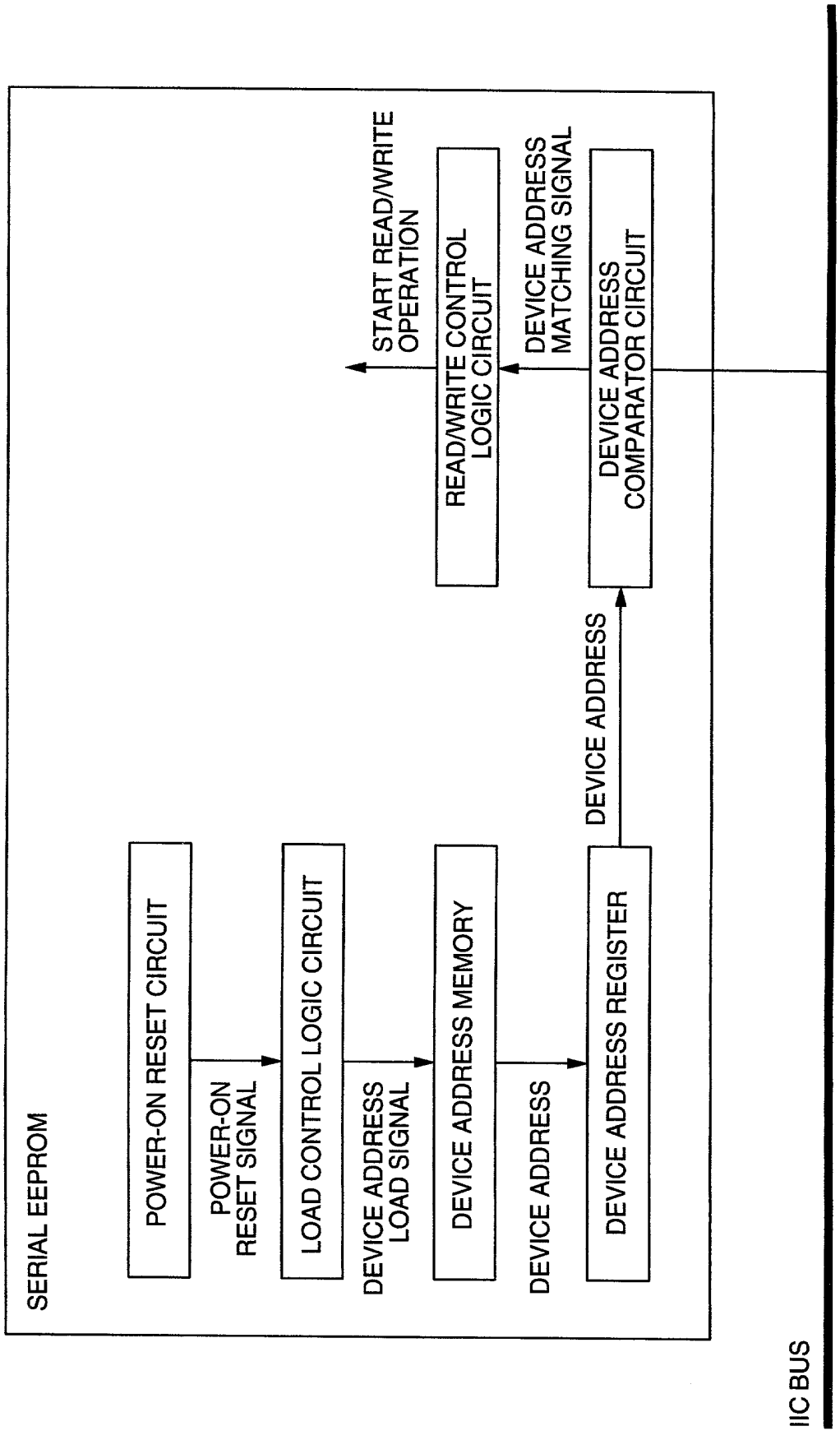


FIG. 5

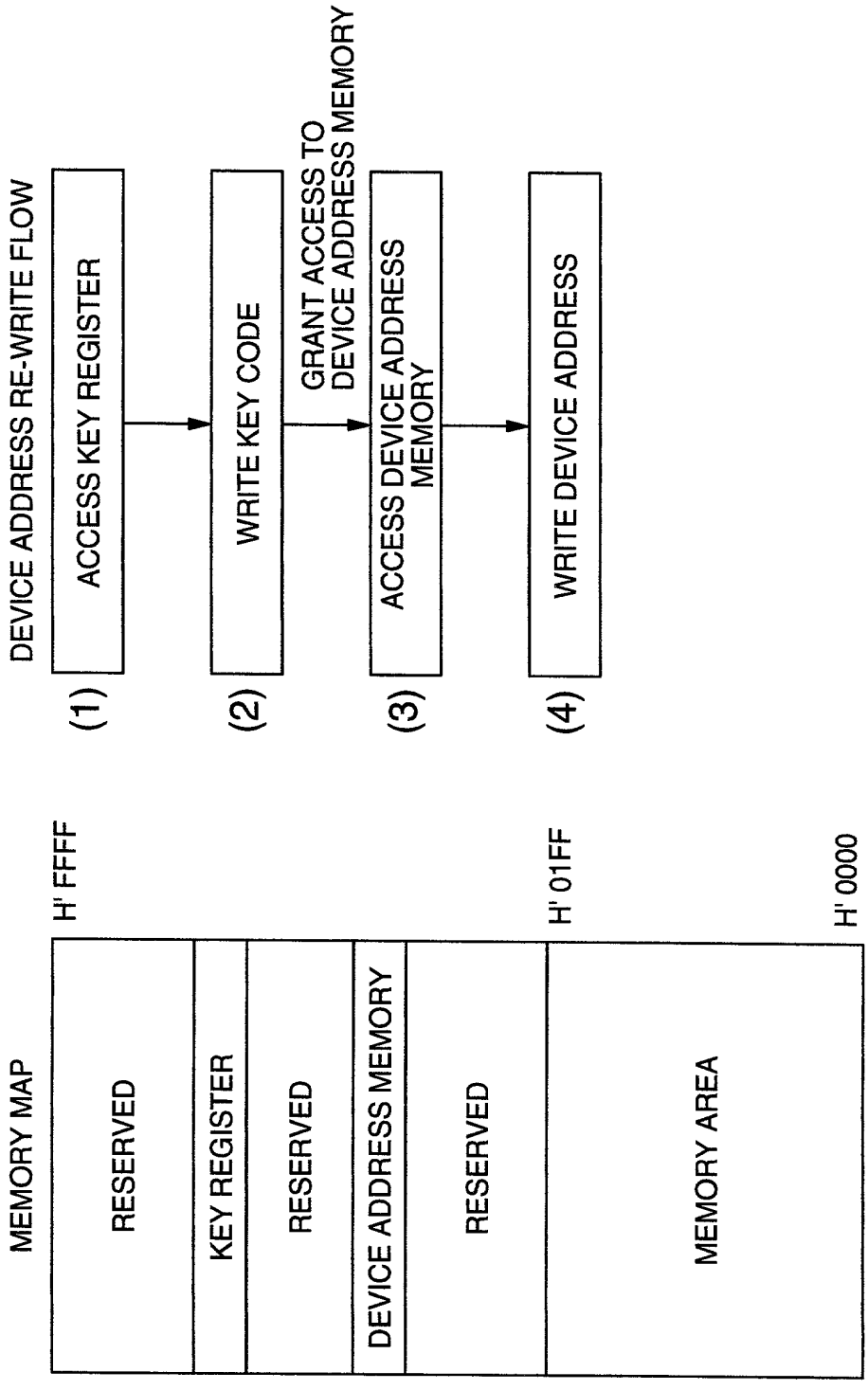

DEVICE ADDRESS RE-WRITE FLOW
(1)
ACCESS KEY REGISTER
(2)
WRITE KEY CODE
GRANT ACCESS TO DEVICE ADDRESS MEMORY
(3)
ACCESS DEVICE ADDRESS MEMORY
(4)
WRITE DEVICE ADDRESS
MEMORY MAP
H' FFFF
RESERVED
KEY REGISTER
RESERVED
DEVICE ADDRESS MEMORY
RESERVED
H' 01FF
MEMORY AREA
H' 0000

FIG. 6

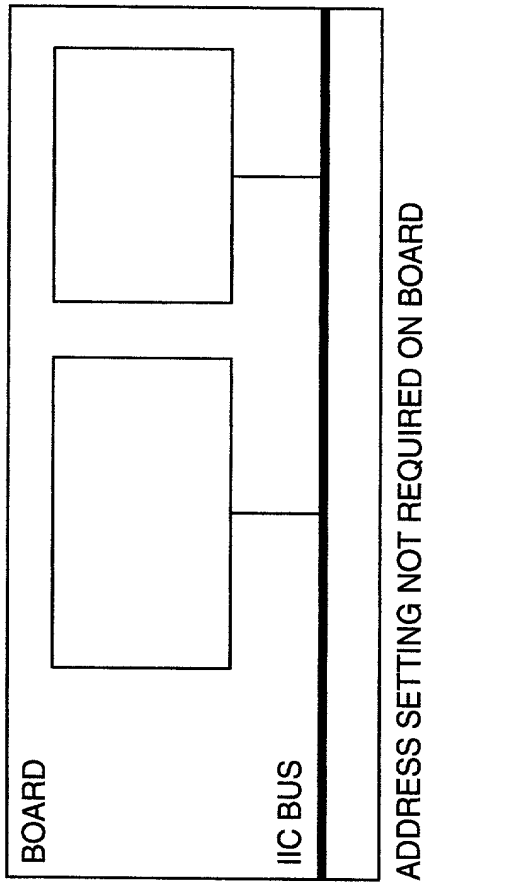
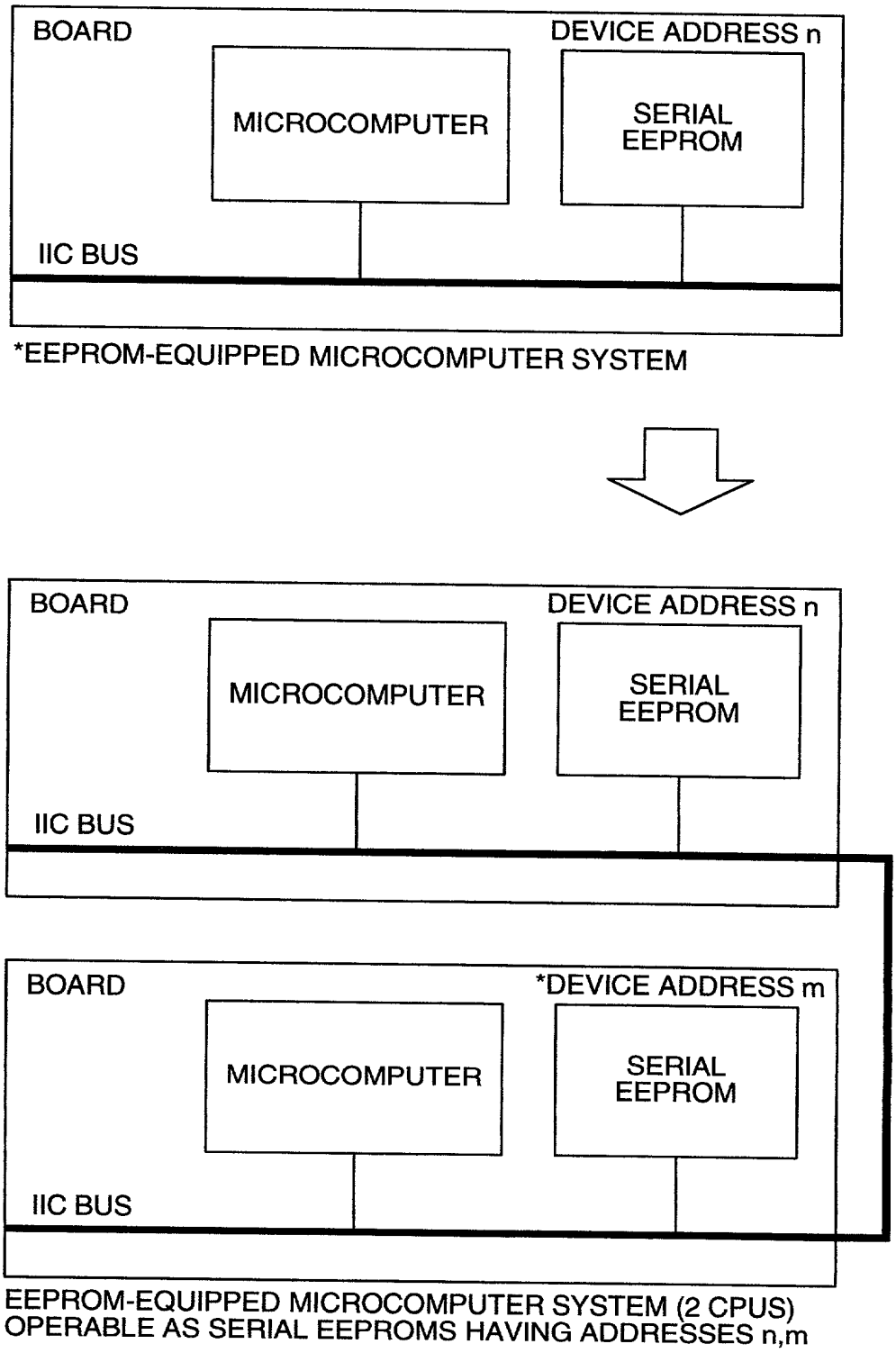

BOARD
IIC BUS
ADDRESS SETTING NOT REQUIRED ON BOARD
MICROCOMPUTER
IIC INTERFACE CONTAINED
SERIAL EEPROM
DEVICE ADDRESS SET TO n

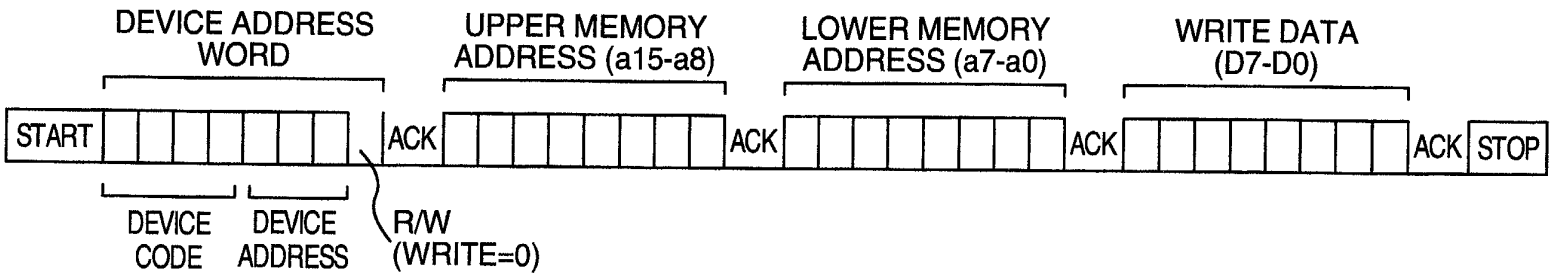
FIG. 7


BOARD
DEVICE ADDRESS n
MICROCOMPUTER
SERIAL EEPROM
IIC BUS
*EEPROM-EQUIPPED MICROCOMPUTER SYSTEM
BOARD
DEVICE ADDRESS n
MICROCOMPUTER
SERIAL EEPROM
IIC BUS
BOARD
*DEVICE ADDRESS m
MICROCOMPUTER
SERIAL EEPROM
IIC BUS
EEPROM-EQUIPPED MICROCOMPUTER SYSTEM (2 CPUS)
OPERABLE AS SERIAL EEPROMS HAVING ADDRESSES n,m

TOH021 "tE030303T

FIG. 8

COMMUNICATION PROTOCOL (FOR WRITE OPERATION)



COMMUNICATION PROTOCOL (FOR READ OPERATION)

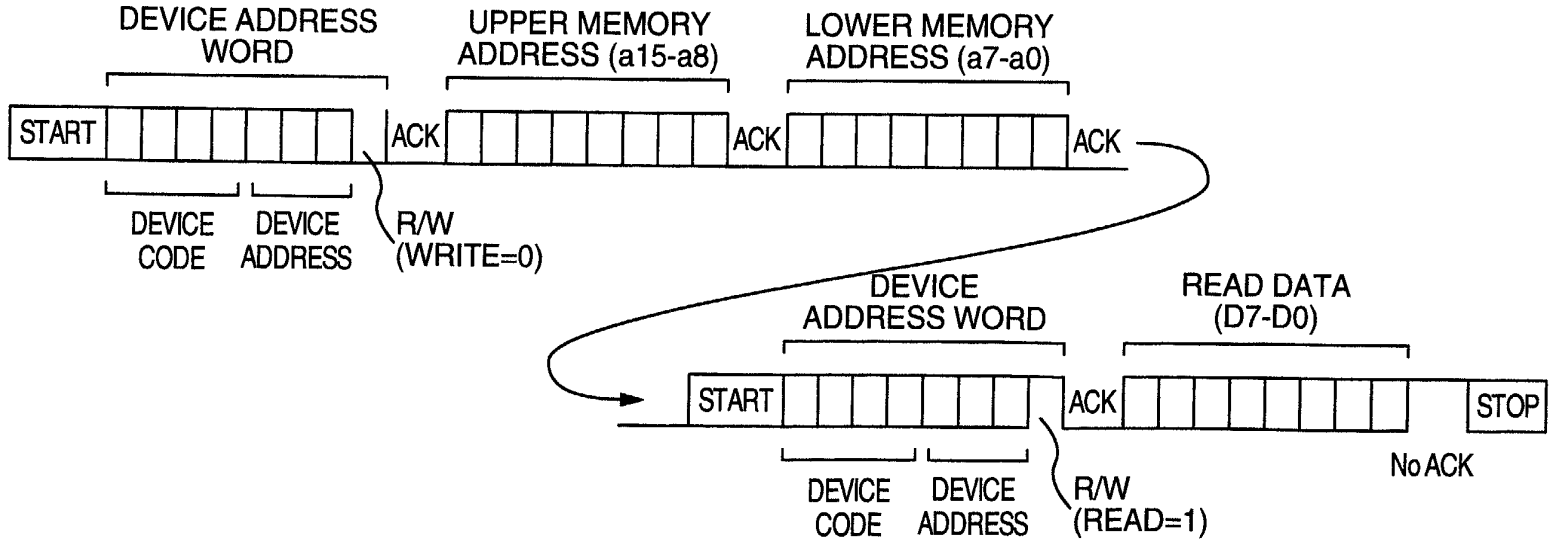
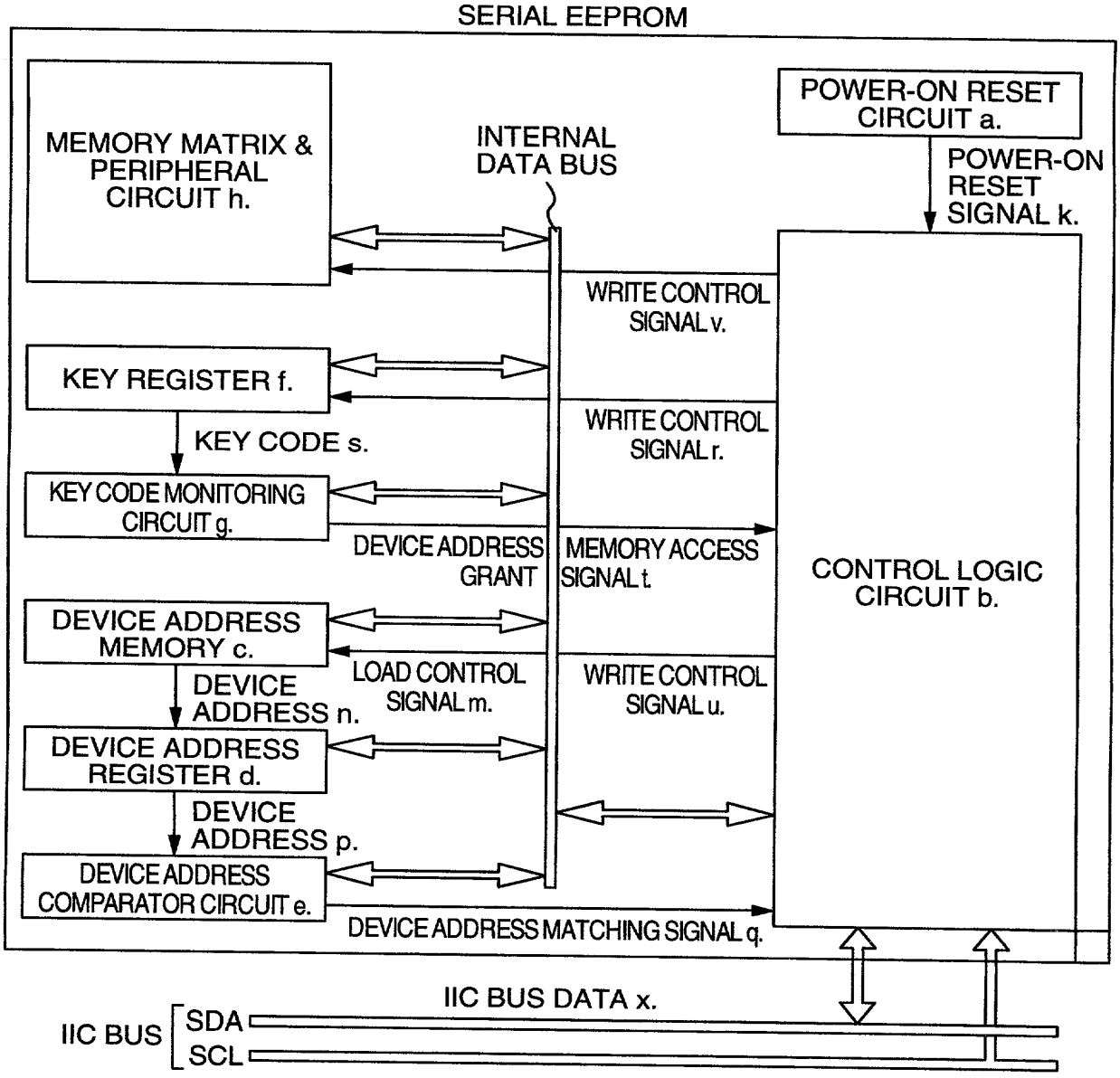


FIG. 9



IIC BUS DATA x.	DEVICE ADDRESS WORD*	UPPER MEMORY ADDRESS	LOWER MEMORY ADDRESS	WRITE DATA
1	10100000	H' FF	H' 10	KEY CODE
2	10100000	H' FF	H' 09	xxxxx101
3	10101010	H' 00	H' 00	WRITE DATA

FIG.10

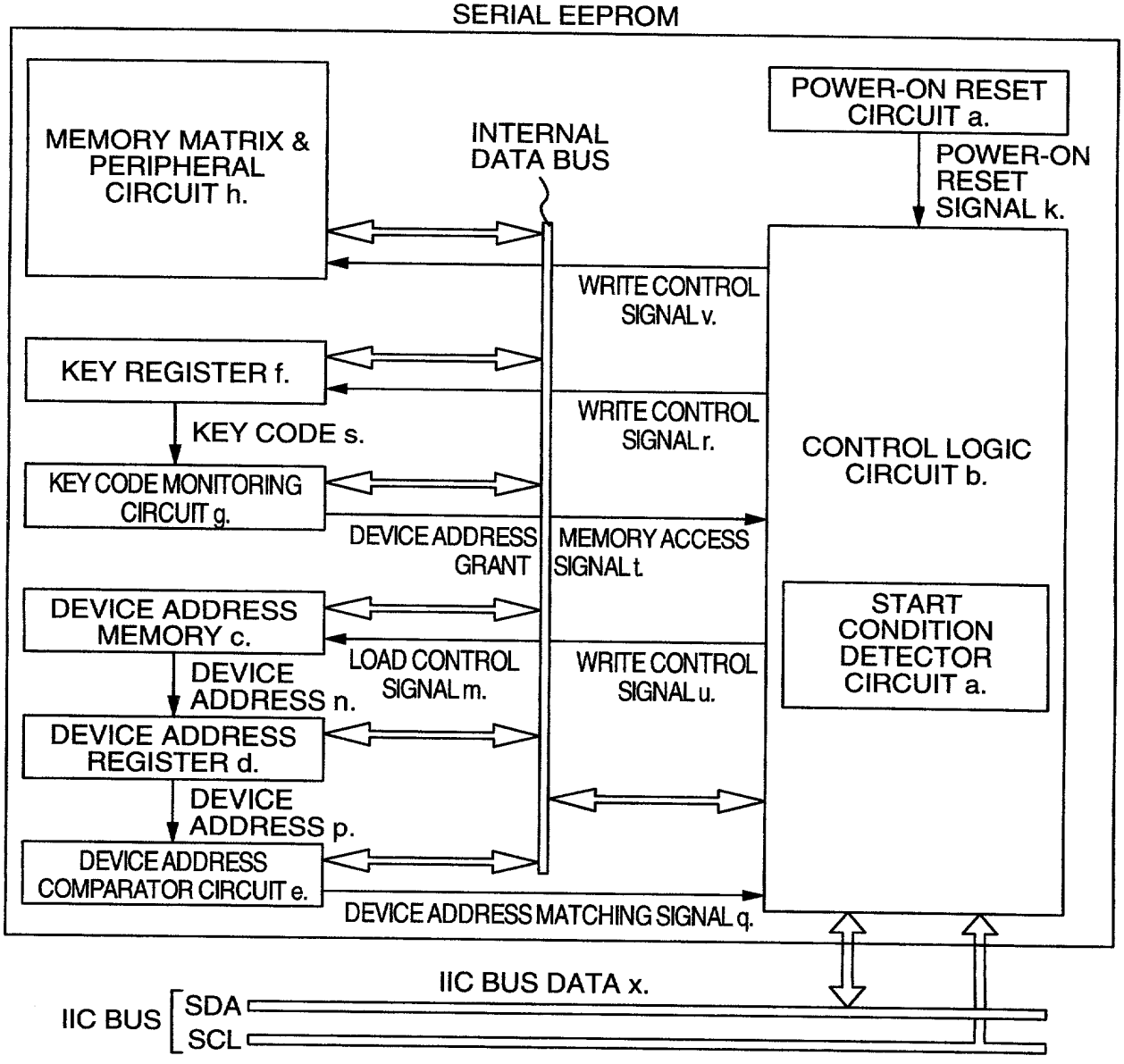
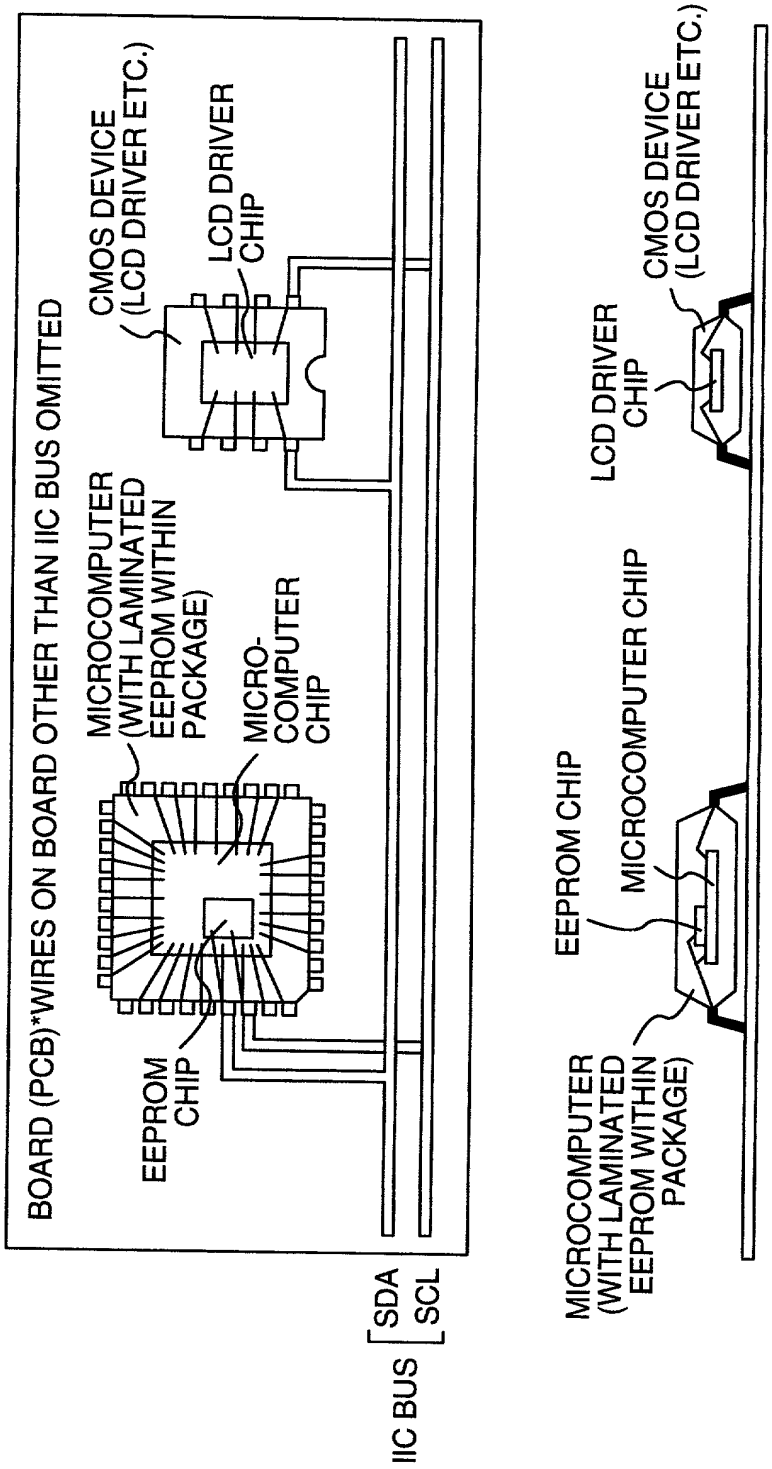
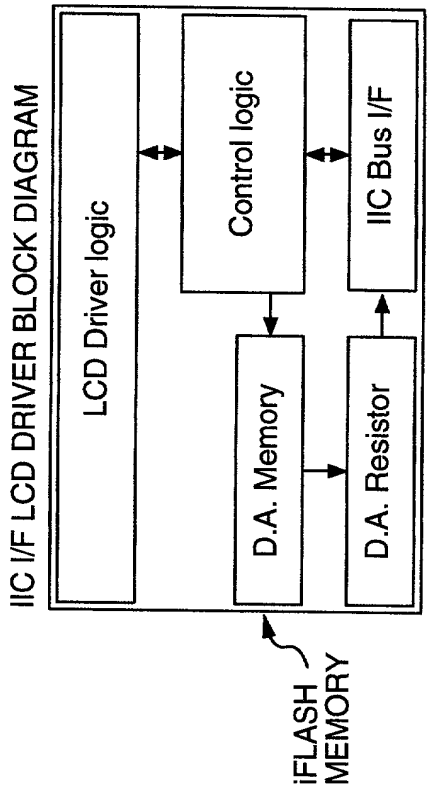

SERIAL EEPROM
MEMORY MATRIX & PERIPHERAL CIRCUIT h.
INTERNAL DATA BUS
POWER-ON RESET CIRCUIT a.
POWER-ON RESET SIGNAL k.
WRITE CONTROL SIGNAL v.
KEY REGISTER f.
WRITE CONTROL SIGNAL r.
KEY CODE s.
CONTROL LOGIC CIRCUIT b.
KEY CODE MONITORING CIRCUIT g.
DEVICE ADDRESS GRANT
MEMORY ACCESS SIGNAL t.
DEVICE ADDRESS MEMORY c.
START CONDITION DETECTOR CIRCUIT a.
LOAD CONTROL SIGNAL m.
WRITE CONTROL SIGNAL u.
DEVICE ADDRESS n.
DEVICE ADDRESS REGISTER d.
DEVICE ADDRESS p.
DEVICE ADDRESS COMPARATOR CIRCUIT e.
DEVICE ADDRESS MATCHING SIGNAL q.
IIC BUS DATA x.
IIC BUS
SDA
SCL

FIG. 11


BOARD (PCB)*WIRES ON BOARD OTHER THAN IIC BUS OMITTED
CMOS DEVICE (LCD DRIVER ETC.)
LCD DRIVER CHIP
MICROCOMPUTER (WITH LAMINATED EEPROM WITHIN PACKAGE)
MICRO-COMPUTER CHIP
EEPROM CHIP
IIC BUS
SDA
SCL
EEPROM CHIP
MICROCOMPUTER CHIP
LCD DRIVER CHIP
CMOS DEVICE (LCD DRIVER ETC.)
MICROCOMPUTER (WITH LAMINATED EEPROM WITHIN PACKAGE)


IIC I/F LCD DRIVER BLOCK DIAGRAM
LCD Driver logic
Control logic
IIC Bus I/F
D.A. Memory
D.A. Resistor
iFLASH MEMORY

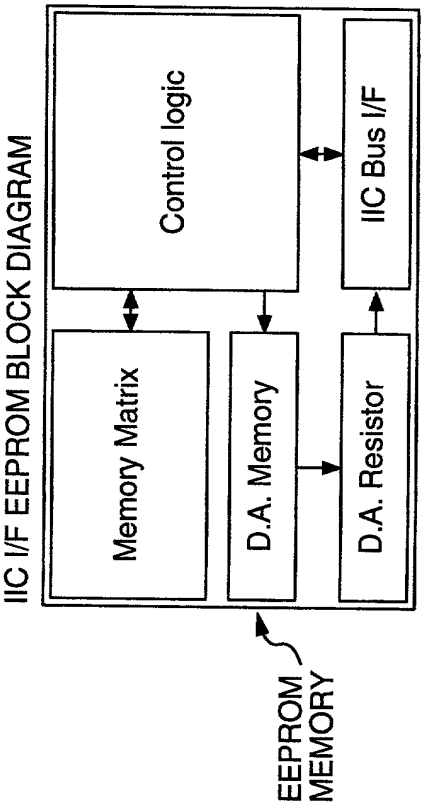
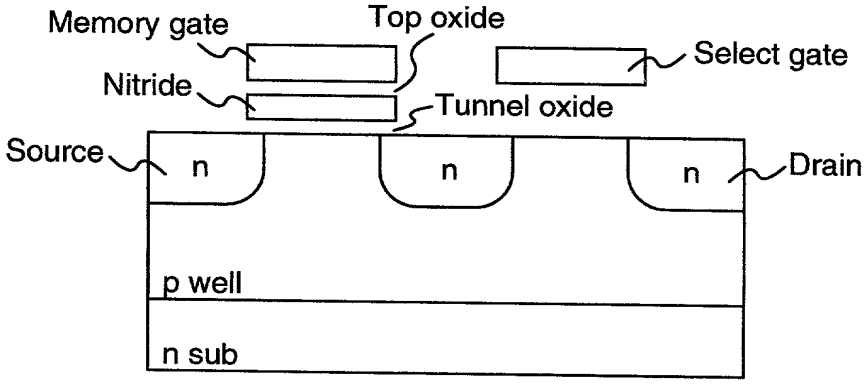

IIC I/F EEPROM BLOCK DIAGRAM
Memory Matrix
Control logic
IIC Bus I/F
D.A. Memory
D.A. Resistor
EEPROM MEMORY

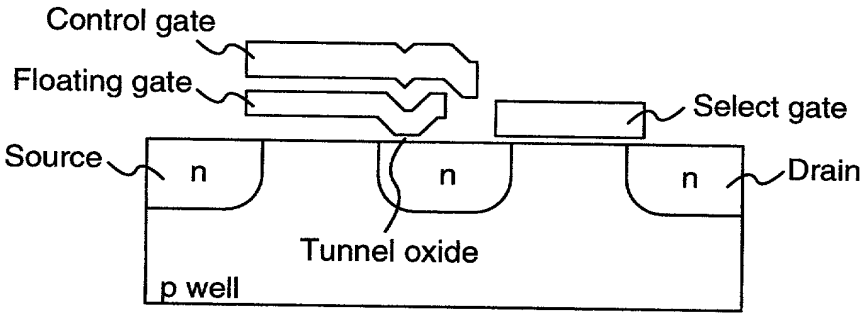
FIG. 12

FIG. 13

MONOS MEMORY CELL



FLOTOX MEMORY CELL



iFLASH MEMORY CELL

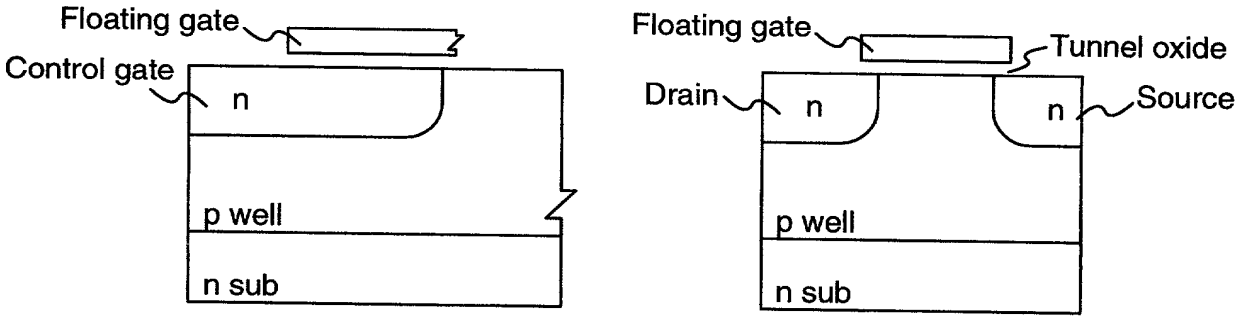


FIG. 14

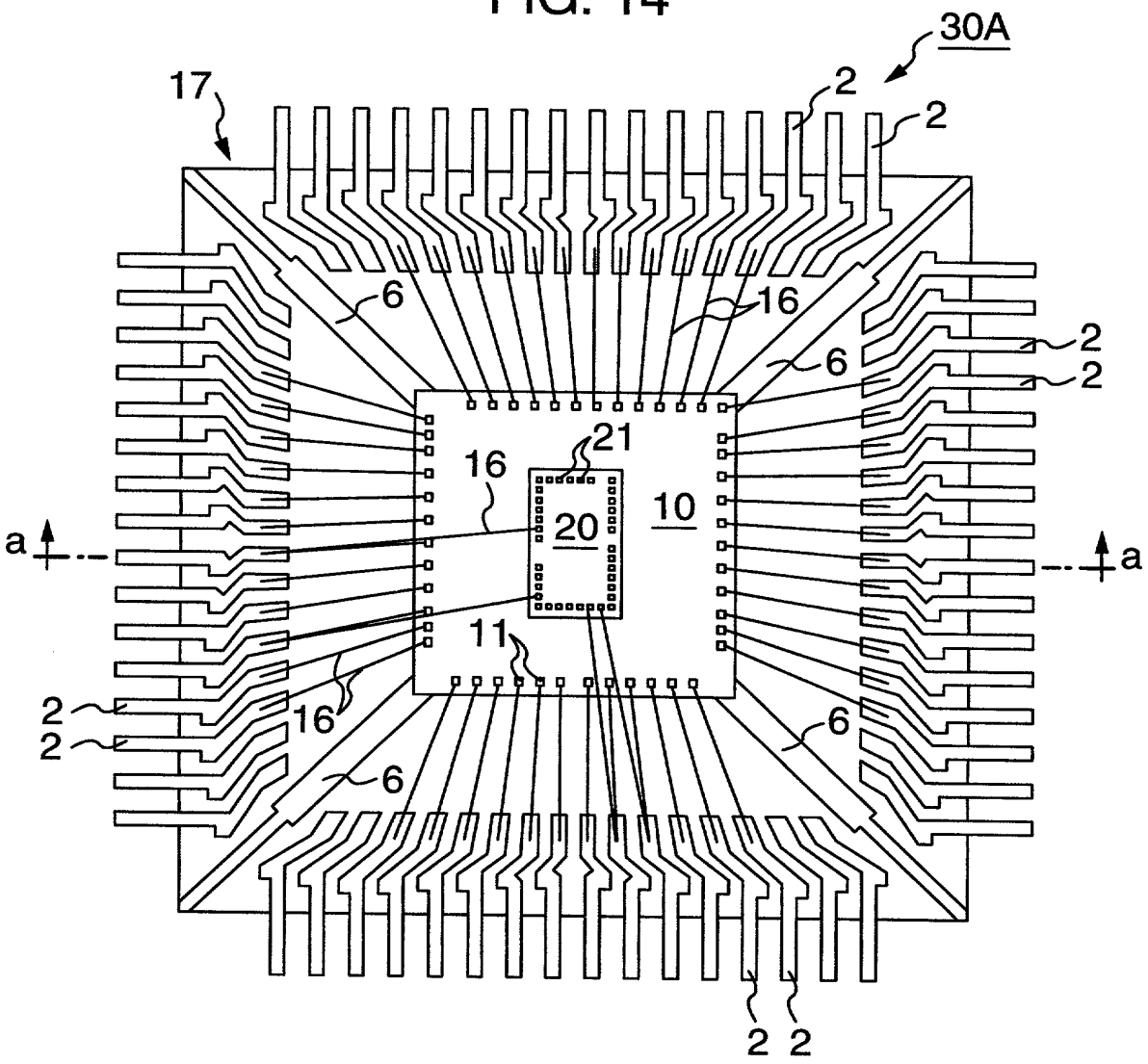


FIG. 15

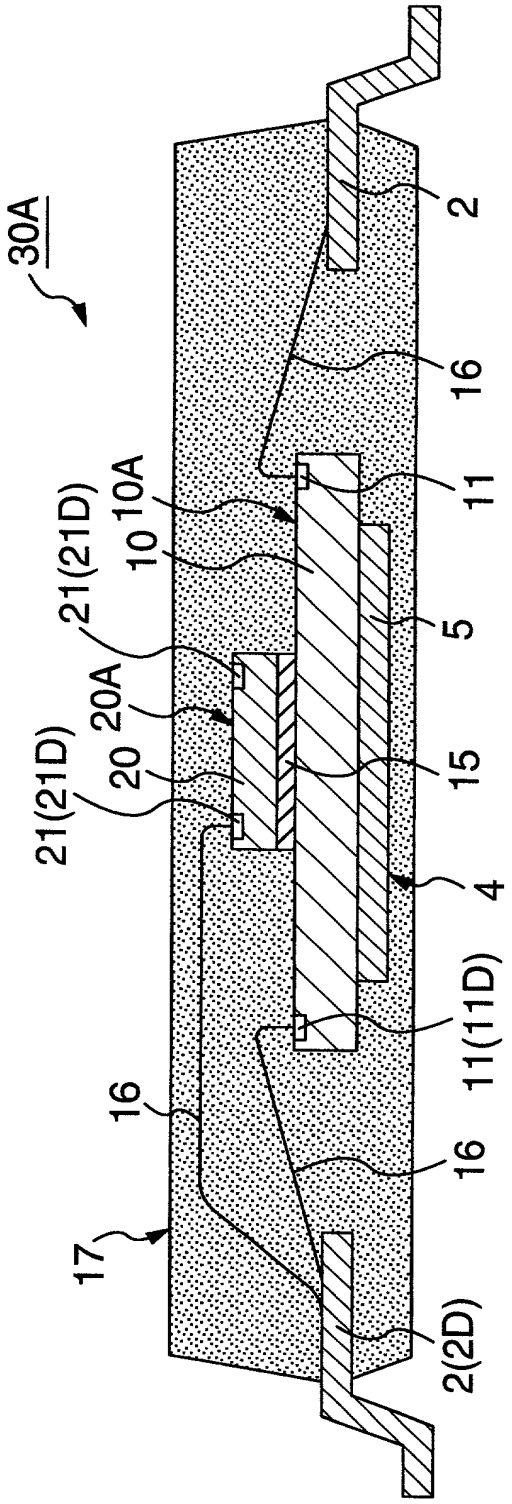


FIG. 16

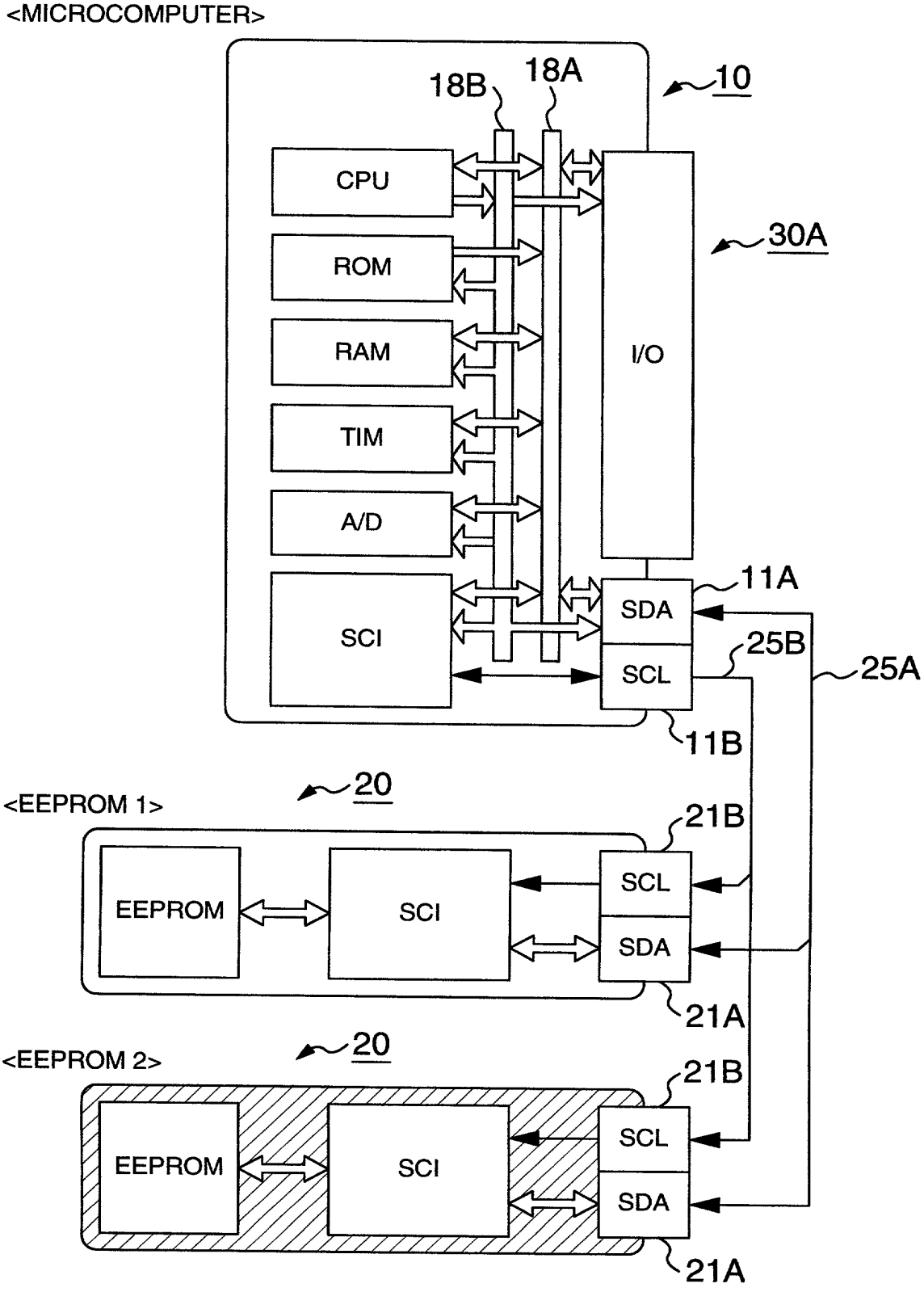

<MICROCOMPUTER>
18B
18A
10
CPU
ROM
RAM
TIM
A/D
SCI
I/O
30A
SDA
SCL
11A
25B
25A
11B
<EEPROM 1>
20
21B
EEPROM
SCI
SCL
SDA
21A
<EEPROM 2>
20
21B
EEPROM
SCI
SCL
SDA
21A

FIG. 17

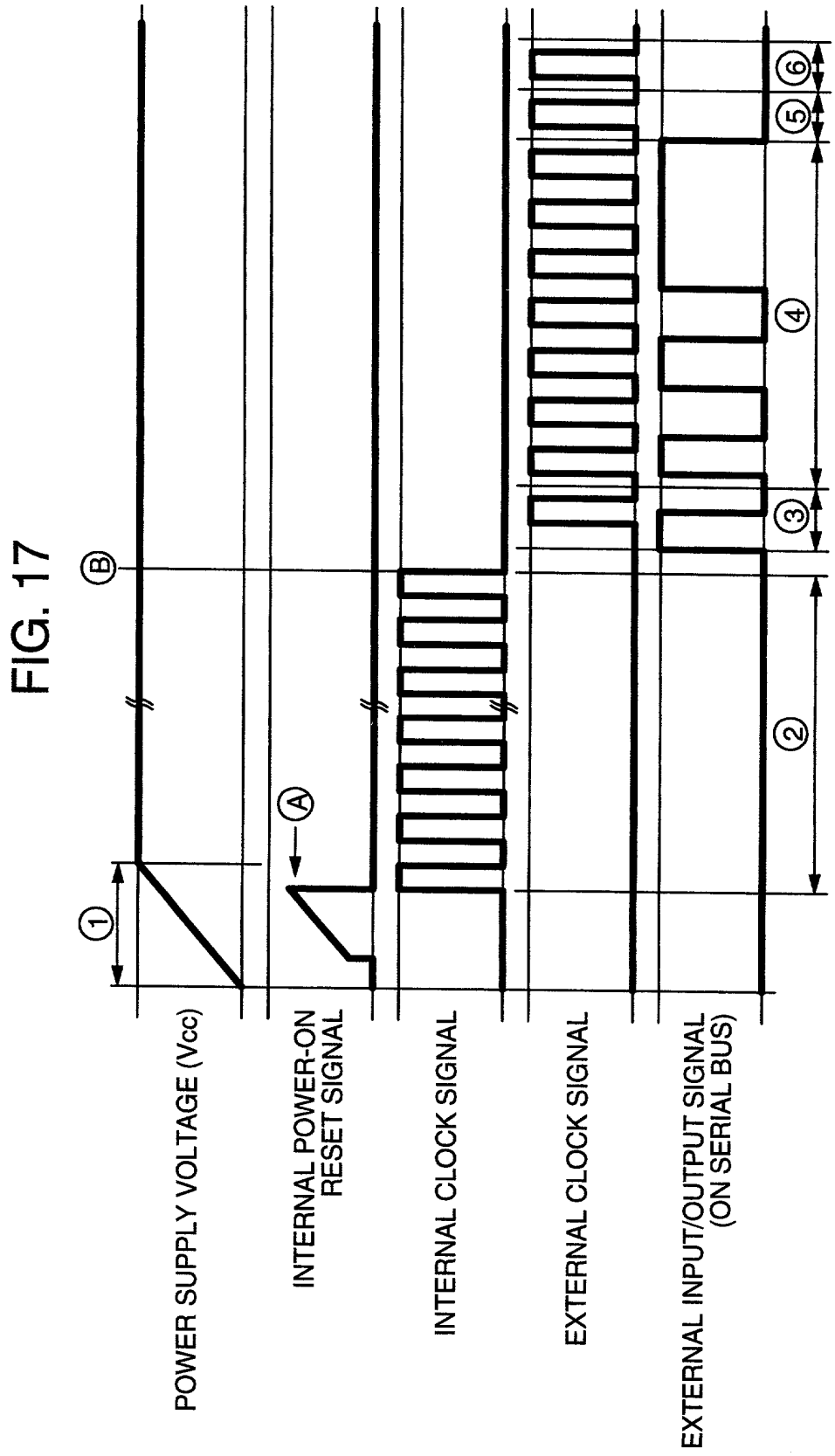

POWER SUPPLY VOLTAGE (Vcc)
INTERNAL POWER-ON RESET SIGNAL
INTERNAL CLOCK SIGNAL
EXTERNAL CLOCK SIGNAL
EXTERNAL INPUT/OUTPUT SIGNAL (ON SERIAL BUS)
①
②
③
④
⑤
⑥
Ⓐ
Ⓑ

FIG. 18

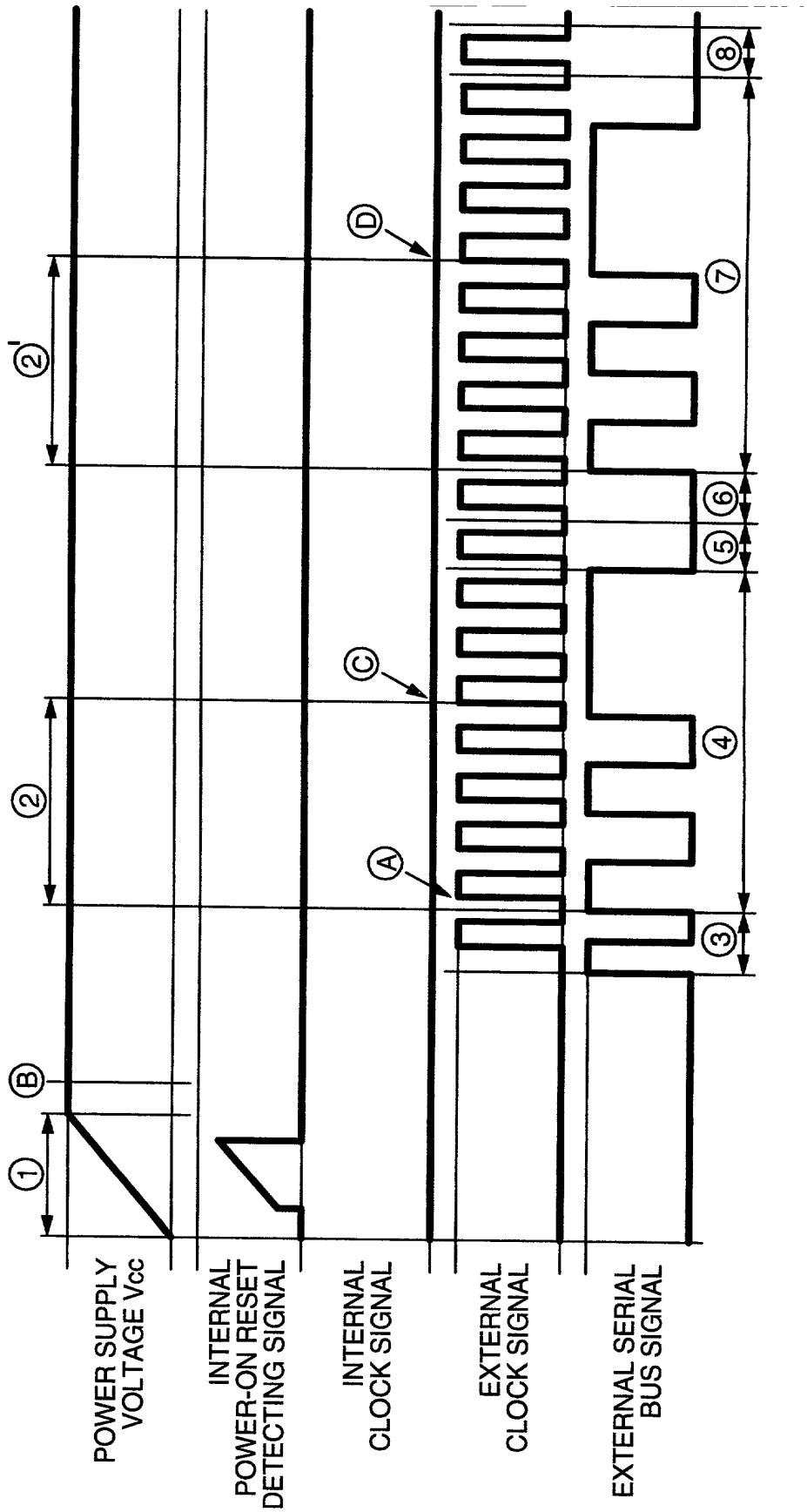
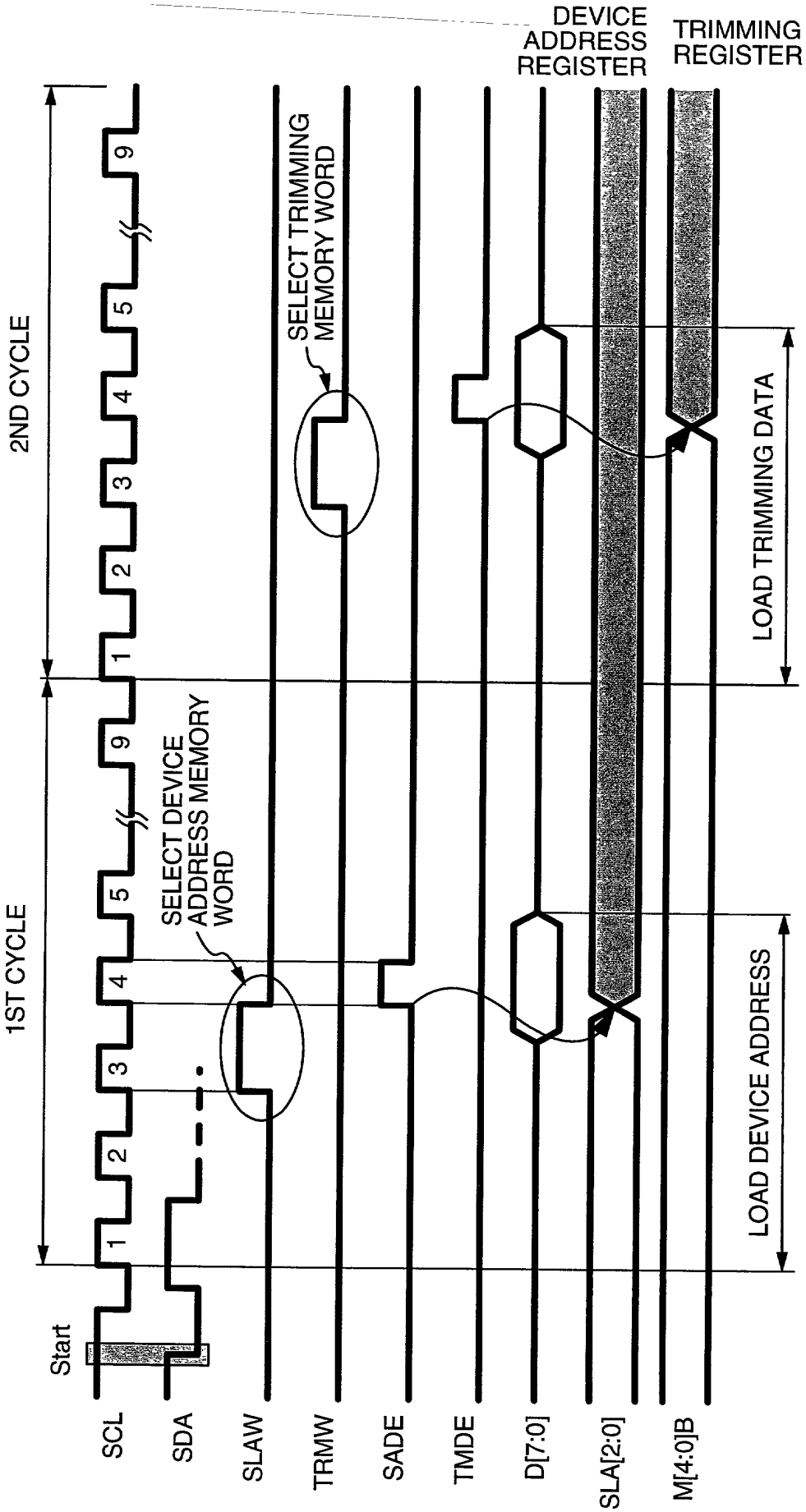

①
②
②'
③
④
⑤
⑥
⑦
⑧
Ⓐ
Ⓑ
Ⓒ
Ⓓ
POWER SUPPLY VOLTAGE Vcc
INTERNAL POWER-ON RESET DETECTING SIGNAL
INTERNAL CLOCK SIGNAL
EXTERNAL CLOCK SIGNAL
EXTERNAL SERIAL BUS SIGNAL

FIG. 19


DEVICE ADDRESS REGISTER
TRIMMING REGISTER
2ND CYCLE
1ST CYCLE
SELECT TRIMMING MEMORY WORD
SELECT DEVICE ADDRESS MEMORY WORD
LOAD TRIMMING DATA
LOAD DEVICE ADDRESS
Start
SCL
SDA
SLAW
TRMW
SADE
TMDE
D[7:0]
SLA[2:0]
M[4:0]B